sensing device for sensing a charge flowing therebetween and a memory cell at the crossing of the former and activated word line, whereafter two consecutive reads of the memory cell are performed and integrated over predetermined time periods in order to generate first and second read values which are compared for determining a logical value dependent on the sensed charge. --

IN THE CLAIMS:

Please cancel claims 7 without prejudice or disclaimer.

Please amend claims 1-6 as follows:

1. (Amended) A sensing device for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors, wherein said sensing device senses a current response corresponding to the data including a binary one or a binary zero, and performs an integration of two read values, the sensing device comprises an integrator circuit for sensing the current response and means for storing and comparing two consecutive read values, one of which is a reference value.

2. (Amended) A sensing device according to claim 1, wherein the integrator circuit comprises an operational amplifier and a capacitor connected between an inverting input of the operational amplifier and the output thereof.

3. (Amended) A sensing device according to claim 2, wherein the integrator circuit comprises a switch connected in parallel over the capacitor.

4. (Amended) A sensing device according to claim 1, wherein the means for two consecutive reads comprises a first sample/hold circuit for sampling/storing a first read value, a second sample/hold circuit for sampling/storing a second read value, and a comparator circuit connected to the outputs of the sample/hold circuits for determining the state of an addressed memory cell.

5. (Amended) A sensing device according to claim 4, wherein the sample/hold circuits comprise capacitors.

6. (Amended) A sensing device according to claim 4, wherein the comparator circuit is an operational amplifier.

[Please add new claim 10 as follows:]

--10. A sensing device for reading data stored in a passive matrix memory comprising memory cells in the form of ferroelectric capacitors, wherein said sensing device senses a

current response corresponding to the data including a binary one or a binary zero, and performs an integration of two read values,

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the sensing device comprises an integrator circuit for sensing the current response and means for storing and comparing two consecutive read values, one of which is a reference value, the means for two consecutive reads comprises a first sample/hold circuit for sampling/storing a first read value, a second sample/hold circuit for sampling/storing a second read value, and comparator circuit connected to the outputs of the sample/hold circuits for determining the sate of an addressed memory cell, a correction circuit being connected between the second sample/hold circuit and the output of the integrator circuit. --